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GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/008,872	LIN ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,11-17 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,11-17,20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-22 have been presented for examination in this application. In response to the last office action, claims 2,8-10,18-19 have been canceled. As the result, claims 1,3-7,11-17,20-22 are pending in this application.

Claims 1,3-7,11-17,20-22 are rejected.

Applicant's remarks filed 3/1/07 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained and restated below,

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1;3,5-7,11-17,20,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 2002/0183013), in view of Chisholm et al (US 5968143), and further in view of Micalizzi Jr, et al (US 6434630).

As for claim 1, Auckland discloses a wireless transceiver device, comprising: modulation circuitry for modulating and demodulating signals that are transmitted over the airwaves (Fig 1: #100); frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals (Fig 1: #100); digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog (Fig 1: #100) (The RF/IF section 104 includes a receive module 110, a transmit module 112 and a frequency synthesizer 114. The receive module 110 generally includes a low noise amplifier (LNA), frequency downconversion, filtering, demodulation, analog to analog to digital conversion, etc., as indicated in FIG. 1.The transmit module 112 generally includes a frequency upconversion, filter, digital to analog conversion and modulation as indicated in FIG. 1;Auckland's paragraph 4, lines 1-8); a radio controller (Fig 1: #100) (The radio 100 includes a digital or baseband section 102, a radio frequency-to-intermediate frequency (RF/IF) section 104 and a radio frequency (RF) section 106;Auckland's paragraph 2, lines 1-2); and baseband processing circuitry including a first in first out memory structure for storing addresses for accessing data block. Auckland discloses a digital signal processor (Fig: 6: #614) to further process the baseband signal into digital packets. Auckand's paragraph 3 discloses that the base band section includes processor and memory elements to store receiving data/commands, to process these data/commands (see Aukland's paragraph 90) and transmitting data/commands to Fig 6: #616 Tx module. Auckland does not disclose the claim's detail of associating data structures to store data/commands in the baseband section as recited in the claim. However, Chisholm discloses a method to transfer data and command blocks between two sides (Chisholm 's Fig 3: host side and memory side), including a FIFO for storing addresses for accessing data blocks (Chisholm 's

Fig 3: #311 registers set (i.e corresponding to the claim's FIFO) for storing command block address of each of the command block from host 103, column 5 lines 25-41), a plurality of command blocks formed with a memory structure, the command blocks include address of data blocks stored within random access memory (Chisholm's column 5 lines 25-39 creating/allocating command address queue portion (corresponding to the claim's command blocks), each command address queue associating with a register in the register set), and a memory portion storing an indicator for indicating whether a command block of the plurality of command block is in use (Chisholm's column 5 lines 30-34, host stores a transfer start signal/bit into the host command address register that corresponding to the command address queue portion, the start signal thus indicates the queue portion is in used). It would have been obvious to one of ordinary skill in the art at the time of invention to include the data structures and method as suggested by Chisholm in Auckland's system, thereby command/data blocks can be transferred quickly in an automatic manner by DMA circuit, eliminating overhead, without any further intervening from local and host processing units (Chisholm's column 5 lines 50-57).

Aukland and Chrisholm do not expressly disclose the command block structure that comprises addresses for accessing data blocks. However, Micalizzi discloses a command block structure having pointers that point to address of associating data segment (Micalizzi's column 8 lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure as suggested by Micalizzi in Auckland's system, thereby separate memory segment that storing data can be easily linked to the a particular command block associating with a particular host's I/O request (Micalizzi's column 8 lines 13-21; Chisholm's column 5 lines 50-57).

As in claim 3, Chrishold discloses wherein the FIFO memory structure includes pointers that defines address of command block (Chisholm's column 5 lines 23-26 discloses creating command block address and associating command block address to the register in register set);

As for claim 5, Auckland discloses wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry (The radio may support any type of carrier modulation such as frequency modulation (FM), gaussian phase shift keying (GPSK), gaussian mean shift keying (GMSK), quadraduture amplitude modulation (QAM) or other scheme now know or later developed; Auckland's paragraph 147, lines 2-4).

As for claim 6, Auckland discloses wherein the frequency conversion circuitry converts directly between radio frequency and baseband (Auckland's paragraph 76, lines 10-12 discloses an ACU capable of tuning to operate at different frequencies; Frequency information comes from baseband processor (Fig 6, DSP #614); The ACU 606 receives frequency, timing, and possibly other control signals at an input 628 from the synthesizer 612, or from the controller 614 as indicated by the dashed line in the drawing figure).

As in claim 7, the claim rejected based on the same rationale as in claim 1. Micalizzi further discloses storing a data block in random access memory (Micalizzi's column 8 lines 40-42).

As in claim 11, Michalizzi discloses address for a data block is only stored in a command block that being stored obviously to an available queue entries (Michalizzi's column 40-45). Chisholm further teaches that the available queue entries can be easily determined by the transfer start signal/bit (see Chishholm's column 5 lines 30-34).

As in claim 12, Chisholm's column 5 lines 23-26 discloses evaluating the address of a command block address stored within a FIFO pointer (creating command block address and associating command block address to the register in register set);

As in claim 13, Micalizzi discloses examining the content of the command block specified by the pointer to determine a data block address (Micalizzi's Fig 3A command block structures can be easily examined to determine the data block address Fig 3A: 110).

As in claim 14-15, Micalizzi discloses evaluating at least a first memory location of the data block whose address is stored in the command block to determine a data block size; retrieving an amount of data corresponding to the data block size (Micalizzi's Fig 3: data segment length #112, #116, column 8 lines 42-46), the data can easily be retrieved and transmitting that data to a radio modem for transmission over wireless airwave (see Auckland's Fig 6: #616).

As in claim 16, Chisholm's column 5 lines 30-34 clearly suggests when the transferring completed, the start/signal bit will be cleared.

As in claim 17, the claim rejected based on the same rationale as in claim 1.

As in claim 20, Chishholm's column 5 lines 30-34 disclose the defined memory portions for storing the command block indicators are each one bit in length.

As in claim 22, Micalizzi's column 6 lines 1-15 clearly disclose the SCSI command format relates to data transferring to particular devices (LUNs).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 2002/0183013), Chisholm et al (US 5968143), Micalizzi Jr, et al (US 6434630) as applied to claim 17, and in view of Fesas, Jr (US 2002/0009075).

As in claim 21, Auckland, Chishold, Micalizzi do not disclose the claim's specific length of the command block. However, Fesas discloses a command block data structure having length of 4 bytes (Fesas's paragraph 10). It would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure having length of 4 bytes as suggested by Fesas in Auckland's system, thereby the command block can be fit into a word of memory (see Fesas's paragraph's 33 lines 1-6).

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

As to the remarks on pages 5-7 for the rejection of claims 1,3,5-7,11-17,20,22 under 35 U.S.C. 103 (a),

A) Regarding Applicant's remarks on page 5 second paragraph, it is noted Aukland teaches the wireless transceiver device as claimed, having **baseband processing circuitry including a first in first out memory structure** for storing addresses for accessing data block. Auckland discloses a digital signal processor (Fig: 6: #614) to further process the baseband signal into digital packets. Auckand's paragraph 3 **discloses that the base band section includes**

processor and memory elements to store receiving data/commands, to process these data/commands (see Aukland's paragraph 90) and transmitting data/commands to Fig 6: #616 Tx module.

Auckland does not expressly disclose the claim's detail of associating data structures for storing data/commands as recited in the claim. That is the limitation "..a FIFO memory structure for storing addresses for accessing data block..".

However, Chisholm discloses a method to transfer data and command blocks between two sides (Chisholm 's Fig 3: host side and memory side), including a FIFO for storing addresses for accessing data blocks (Chisholm 's Fig 3: #311 registers set (i.e corresponding to the claim's FIFO) for storing command block address of each of the command block from host 103, column 5 lines 25-41). Chisholm further teaches that the command block for example can be the command block for transferring command and data for SCSI device (see Chisholm's column 4 lines 25-37), Chisholm further discloses **data corresponding to** such SCSI command/command block **is stored in memory Fig 3: #203** (see Chisholm's column 4 lines 52-56), Chisholm further discloses that the DMA state machine **handle data blocks transferring** in and out of memory #203 (see Chisholm's column 5 lines 8-11).

Therefore in contrast to Applicant's remarks on page 6, Chisholm device executing the command block and data block transferring operations.

B) Regarding Applicant's remark "the dissimilar command blocks of Chisholm do not include **addresses of data blocks** stored within random access memory". Firstly, it is noted the claim's limitation merely required "address for accessing data block" and not requiring addresses of data blocks as Applicant's remark. Secondly, Examiner disagrees with Applicant's

characterization of Chisholm's command block. As discussed in item A, Chisholm discloses the command block for example can be the command block for transferring command and data for SCSI device (see Chisholm's column 4 lines 25-37). Although Auckland and Chisholm do not expressly disclose the detail structure of the command block, for example a detail structure of a SCSI command block. However, Micalizzi clearly discloses the detail structure of the SCSI command block that includes addresses for data transferring operation (see Micalizzi's Fig 3A: #110, #116 data segments 0,1 addresses).

C) Regarding the claim's limitation of "the command blocks include...and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in used". Examiner maintains that Chisholm discloses Fig 3: #311 registers set for storing command block address of each of the command block from host 103, column 5 lines 25-41. Chisholm's column 5 lines 30-34, further discloses the register set Fig 3: #311 (corresponding to the claim's memory structure) storing a transfer start signal/bit that indicates the command block is in used.

D) Regarding the Applicant's remarks on page 7 second paragraph, as discussed in above paragraphs, Chisholm teaches the a transfer start signal/bit that indicates the command block is in used. That is the start signal/bit indicating for the data associating with the command block has yet to be successfully processed and that the command block is busy.

E) Regarding Applicant's remarks on page 7, fourth paragraph, it's noted that Auckland teaches the typical components of the wireless transceivers device as claimed, such as RF component, modulation circuitry, conversion circuitry to **the baseband component** which has a processing element (DSP processor) to process the command and data for the transceiver device.

Auckland does not describe the detail of memory structures for processing the commands and data. However, Chisholm discloses memory structures for storing the data and commands in memory area such that the processing element can access commands, command blocks and start processing data associating with the commands. It would have been obvious to one of ordinary skill in the art at the time of invention to include the data structures in memory and method as suggested by Chisholm in Auckland's system, thereby command/data blocks can be transferred quickly in an automatic manner by DMA circuit, eliminating overhead, without any further intervening from local and host processing units (Chisholm's column 5 lines 50-57).

Aukland and Chrisholm do not expressly disclose the command block structure that comprises addresses for accessing data blocks. However, Micalizzi discloses a command block structure having pointers that point to address of associating data segment (Micalizzi's column 8 lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure as suggested by Micalizzi in Auckland's system, thereby separate memory segment that storing data can be easily linked to the a particular command block associating with a particular host's I/O request (Micalizzi's column 8 lines 13-21; Chisholm's column 5 lines 50-57). The linked data structures (i.e data blocks, command blocks linking) in memory further allowing the processing element to quickly and efficiently process the commands and associating data blocks in an automatic manner, reducing interruption (i.e overhead processing), and thereby further improve the overall system's throughput.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Kevin L. Ellis
Primary Examiner

4/12/07